WHAT IS CLAIMED IS:

1. A router for interconnecting N interfacing peripheral devices, said router comprising a plurality of routing nodes coupled to one another via switching circuitry, a first one of said plurality of routing nodes comprising:

at least one physical medium device (PMD) module capable of transmitting data packets to and receiving data packets from selected ones of said N interfacing peripheral devices;

an ingress processor capable of receiving incoming data packets from said at least one PMD module;

an egress processor capable of transmitting data packets to said at least one PMD module; and

a medium access control (MAC) processor capable of forwarding data packets from said ingress processor to said switching circuitry and forwarding data packets from said switching circuitry to said egress processor, wherein said MAC processor is capable of determining whether a first data packet received from said ingress processor is directed to said egress processor and, in response to said determination, transferring said first data packet directly to said egress processor without forwarding said first data packet through said switching circuitry.

2. The router as set forth in Claim 1 wherein said MAC processor determines whether said first data packet is directed to said egress processor by an address of said first data packet.

3. The router as set forth in Claim 2 wherein said MAC processor determines that said first data packet is directed to said egress processor if said address of said first data packet matches an address of said MAC processor.

4. The router as set forth in Claim 3 wherein said MAC processor forwards said first data packet to said switching circuitry if said address of said first data packet does not match said address of said MAC processor.

5. The router as set forth in Claim 4 wherein said MAC processor comprises a field programmable gate array.

6. The router as set forth in Claim 5 wherein said MAC processor comprises a transmit state machine capable of capable of determining whether said first data packet is directed to said egress processor.

7. The router as set forth in Claim 6 wherein said MAC processor comprises a receive state machine coupled to said transmit state machine capable of receiving said first data packet from said transmit state machine if said transmit state machine determines said first data packet is directed to said egress processor.

8. The router as set forth in Claim 7 wherein said receive state machine forwards said first data packet from said transmit state machine to said egress processor.

9. A communication network comprising a plurality of routers that communicate data packets to one another and to interfacing peripheral devices, each router comprising a plurality of routing nodes coupled to one another via switching circuitry, wherein a first one of said plurality of routing nodes comprises:

a physical medium device (PMD) module capable of transmitting data packets to and receiving data packets from external devices;

an ingress processor capable of receiving incoming data packets from said PMD module;

an egress processor capable of transmitting data packets to said PMD module; and

a medium access control (MAC) processor for forwarding data packets from said ingress processor to said switching circuitry and forwarding data packets from said switching circuitry to said egress processor, wherein said MAC processor determines whether a first data packet received from said ingress processor is directed to said egress processor and, in response to said determination, transfers said first data packet to said egress processor without forwarding said first data packet through said switching circuitry.

10. The communication network as set forth in Claim 9 wherein said MAC processor determines whether said first data packet is directed to said egress processor by an address of said first data packet.

11. The communication network as set forth in Claim 10 wherein said MAC processor determines that said first data packet is directed to said egress processor if said address of said first data packet matches an address of said MAC processor.

12. The communication network as set forth in Claim 11 wherein said MAC processor forwards said first data packet to said switching circuitry if said address of said first data packet does not match said address of said MAC processor.

13. The communication network as set forth in Claim 12 wherein said MAC processor comprises a field programmable gate array.

14. The communication network as set forth in Claim 13 wherein said MAC processor comprises a transmit state machine capable of capable of determining whether said first data packet is directed to said egress processor.

15. The communication network as set forth in Claim 14 wherein said MAC processor comprises a receive state machine coupled to said transmit state machine capable of receiving said first data packet from said transmit state machine if said transmit state machine determines said first data packet is directed to said egress processor.

16. The communication network as set forth in Claim 15 wherein said receive state machine forwards said first data packet from said transmit state machine to said egress processor.

17. For use in a router comprising a plurality of routing nodes coupled to one another via switching circuitry, a method of forwarding data packets comprising the steps of:

receiving in an ingress processor a first data packet from an external device;

forwarding the received first data packet to a medium access control (MAC) processor capable of forwarding data packets from the ingress processor to the switching circuitry;

determining in the MAC processor whether the first data packet received from the ingress processor is directed to an egress processor associated with the MAC processor; and

in response to a determination that the first data packet is directed to the egress processor, transferring the first data packet directly to the egress processor without forwarding the first data packet through the switching circuitry.

18. The method as set forth in Claim 17 wherein the step of determining whether the first data packet received from the ingress processor is directed to the egress processor comprises the step of determining whether an address of the first data packet matches an address of the MAC processor.

19. The method as set forth in Claim 18 further comprising the step of forwarding the first data packet to the switching circuitry if the address of the first data packet does not match the address of the MAC processor.

20. The method as set forth in Claim 19 wherein the step of transferring the first data packet directly to the egress processor comprises the sub-step of forwarding the first data packet to the egress processor if the address of the first data packet matches the address of the MAC processor.